Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **ILIM**
2. **FB**
3. **COMP**
4. **SS/SD**
5. **GND**
6. **GND**
7. **LDRV**
8. **VDD**
9. **VDD**
10. **SW**
11. **HDRV**
12. **BOOT**

**.060”**

**.062”**

**1**

**2**

**3**

**4**

**5**

**6**

**12**

**11**

**10**

**9**

**8**

**7**

**MASK**

**REF**

**TPS40001AA**

**Top Material: CuNiPd**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: FLOAT**

**Mask Ref: TPS40001AA**

**APPROVED BY: DK DIE SIZE .060” X .062” DATE: 4/27/23**

**MFG: TEXAS INSTRUMENTS THICKNESS .015” P/N: TPS40007**

**DG 10.1.2**

#### Rev B, 7/1